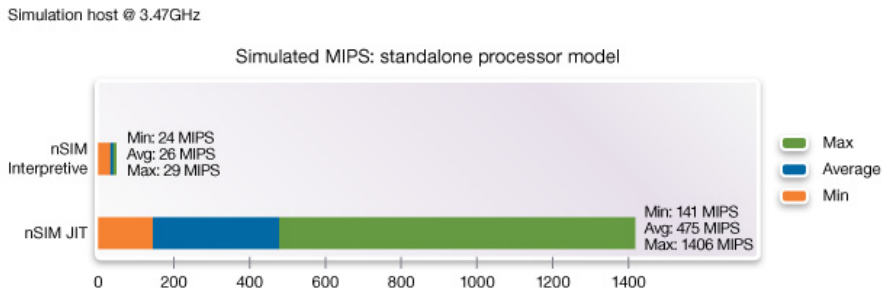
# DesignWare ARC nSIM

The DesignWare® ARC™ nSIM Instruction Set Simulator provides an instruction accurate processor model for the DesignWare ARC processor families. Such processor models take the software development out of your products' critical path by enabling an early start as well as increased efficiency through enhanced visibility and control. The nSIM models provide a complete and accurate hardware/software interface model of the ARC processors that guarantees binary compatibility of product code between the simulation platform and the hardware. The model is configurable and supports all the ARC processor families, ranging from the deeply embedded ARC EM family to the general purpose ARC 600 family, the ARC 700 family for high-performance applications, as well as the ARC AS200 audio processors.

The nSIM model comes with a state-of-the-art JIT compilation engine that leverages the capabilities of multi-core simulation hosts by offloading JIT translation threads from the core that is running the simulation reducing the JIT compilation overhead and significantly speeding up simulation performance. Embedded Microprocessor Benchmark Consortium (EEMBC) benchmarks on a simulation host running at 3.47 GHz show an 18X speed increase, on average, when JIT mode is activated and JIT translation is offloaded to a separate core of the simulation host. As a result, an average performance of 475 MIPS is reached across all 34 tests of the test suite. And over 1,400 MIPS is reached for the EEMBC bezier01 test that benefits most of the JIT activation.




For the ARC EM family, the JIT compilation engine can be combined with an efficient micro-architectural performance model of the ARC processor pipeline. This enables near cycle-accurate simulation with a cycle accuracy of 95% (compared to RTL) at simulation speeds of over 25 MIPS, making it the ideal solution for high-speed architectural exploration and system profiling. In case a full 100% cycle accuracy is needed for the final performance tweaking, it is easy to switch over to the DesignWare ARC xCAM models that are derived from the processor's Verilog to achieve 100% cycle accuracy.

| | Interpretive | JIT | |
|---|---|---|---|
| Instruction\ Register\ Programmers View Accurate (Instruction Set Architecture model) | Base mode Avg. 20 MIPS | Turbo mode Avg. 475 MIPS | SW development and debugging Function and instruction accurate profiling and optimization |
| Near Cycle-Accurate (micro-architectural processor pipeline performance model) | NCAM turbo mode[1] Avg. 25 MIPS, up to 95% Cycle Accuracy | | Cycle Approximate profiling and optimization High-speed Architectural exploration and system profiling and optimization |

[1] While it is possible to run the NCAM Turbo model in Interpretive mode, doing so does not add value as it will only reduce simulation performance without adding accuracy.

**Table 1: DesignWare ARC nSIM offers three modes of operation that you can switch between to balance performance and accuracy depending on the specific demands of your application. Listed performance numbers are average across 34 EEMBC tests, in standalone processor mode operation.**

The nSIM processor model is delivered as a single DLL that integrates seamlessly with the MetaWare and GNU debuggers. Switching between the different operating modes like JIT or NCAM is as easy as invoking the model with the appropriate command-line parameter. The nSIM models come with an industry-standard OSCI TLM-2.0 SystemC interface to support their integration with OSCI standard peripheral models. In addition, the nSIM models implement the required interfaces for deployment in the Synopsys Virtualizer platform, a tool for the creation, assembly and execution of SystemC-based virtual prototypes for pre-silicon software development and software-driven verification.

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DesignWare ARC nSIM Instruction Set Simulator Datasheet

Highlights End User Agreement Products Downloads and Documentation

- Single model supporting the ARC EM, ARC 600, ARC 700 and ARC AS200 families
- Available in standalone mode – for processor centric algorithm development and performance tuning at highest simulation speed
- OSCI TLM-2.0 SystemC standard interface for integration with OSCI standard peripheral models
- Virtualizer integration layer provide access to advanced debugging and profiling capabilities offered by Virtualizer
- Very high speed JIT mode benefits from multi-core simulation hosts: 475 MIPS simulated performance for the EEMBC test suite on the ARC nSIM model for the ARC EM family
- High-speed near cycle-accuracy for system profiling and architectural exploration: up to 95% accuracy compared to RTL at over 25 MIPS (ARC EM family only)
- Seamless switching between different simulation modes by simple debugger command-line invocation
- Available for 32/64 bit Windows and Linux simulation hosts
- Models for EIA processor extensions and custom instructions can be added as an extension DLL or as a separate SystemC component



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